IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
RAYNOR ET AL.

Serial No. **Not Yet Assigned**

Filing Date: **Herewith**

For: **SOLID STATE IMAGING DEVICE**

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EXPRESS MAIL NO: EI747059665US

DATE OF DEPOSIT: November 16, 2001

NAME: Greg French

SIGNATURE:

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for a proposed drawing modification as indicated in red ink to label FIG. 2 as prior art. FIGS. 1-14 are also being to remove extraneous markings therefrom as indicated in red ink.

In the Specification:

Please replace the paragraph beginning at page 4, line 22-29, with the following rewritten paragraph:

-- In view of the foregoing background, this and other objects, advantages and features of the present invention are provided by a solid state imaging device comprising a two-dimensional array of pixels defining an image

plane, and readout electronics comprising at least one store circuit laterally adjacent the image plane for reading signals therefrom in a predetermined manner.

The invention is based upon locating the readout electronics off the image plane of the device. In preferred forms of the invention, this is facilitated by connecting each pixel to its associated readout electronics via a multiconductor signal bus. The readout electronics may be laterally adjacent one side of the image plane, are they may be laterally adjacent opposing sides of the image plane.

Each pixel preferably comprises a photosensitive diode, and a switching circuit for resetting and discharging the diode. The switching circuit may includes a first transistor for applying a reset pulse, and a second transistor for connecting the diode to a conductor within the multiconductor signal bus.

The at least one store circuit preferably comprises a plurality of store circuits, with a store circuit corresponding to each pixel. Each store circuit may comprise a first store circuit for storing a reset value, and a second store circuit for storing a read out value. The read out value of a given pixel may be modified by the stored reset value for that pixel. A third store circuit stores a second reset value, with a current reset value and a current read out value being processed simultaneously based upon application of a new reset pulse. --

In the Claims:

Please cancel Claims 1 to 10.

Please add new Claims 11 to 40.

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11. A solid state imaging device comprising:

a two-dimensional array of pixels defining an image plane; and

readout electronics comprising at least one store circuit laterally adjacent the image plane for reading signals therefrom.

12. A solid state imaging device according to Claim 11, further comprising a multiconductor signal bus connected between said array of pixels and said readout electronics.

13. A solid state imaging device according to Claim 12, wherein each pixel comprises:

a photosensitive diode; and

a switching circuit for resetting and discharging said diode, said switching circuit comprising

a first transistor for applying a reset pulse, and

a second transistor for connecting said diode to a conductor within said multiconductor signal bus.

14. A solid state imaging device according to Claim 11, wherein said multiconductor signal bus comprises a plurality of stacked conductors.

15. A solid state imaging device according to Claim 11, wherein said readout electronics are laterally adjacent one side of the image plane.

16. A solid state imaging device according to Claim

11, wherein said readout electronics are laterally adjacent two opposing sides of the image plane.

17. A solid state imaging device according to Claim 11, wherein all pixels of said array of pixels are reset simultaneously and are read out simultaneously.

18. A solid state imaging device according to Claim 11, wherein said at least one store circuit comprises a plurality of store circuits, with a store circuit corresponding to each pixel and comprising:

a first store circuit for storing a reset value; and

a second store circuit for storing a read out value, with the read out value of a given pixel being modified by the stored reset value for that pixel.

19. A solid state imaging device according to Claim 18, wherein each store circuit further comprises:

a third store circuit for storing a second reset value, with a current reset value and a current read out value being processed simultaneously based upon application of a new reset pulse.

20. A solid state imaging device according to Claim 19, wherein said readout electronics further comprises:

a differential amplifier connected to said first, second and third store circuits; and

a reset circuit for placing said differential amplifier in a common mode reset state prior to reading a signal.

21. A solid state imaging device comprising:

a two-dimensional array of pixels defining an image plane, each pixel comprising a photosensitive diode, and a switching circuit for resetting and discharging said diode;

a signal bus connected to said array of pixels; and

readout electronics comprising at least one store circuit laterally adjacent the image plane and connected to said signal bus for reading signals from said array of pixels.

22. A solid state imaging device according to Claim 21, wherein said signal bus comprises a multiconductor signal bus; and wherein said switching circuit comprises:

a first transistor for applying a reset pulse; and

a second transistor for connecting said diode to a conductor within said multiconductor signal bus.

23. A solid state imaging device according to Claim 21, wherein said signal bus comprises a multiconductor signal bus comprising a plurality of stacked conductors.

24. A solid state imaging device according to Claim 21, wherein said readout electronics are laterally adjacent one side of the image plane.

25. A solid state imaging device according to Claim 21, wherein said readout electronics are laterally adjacent two opposing sides of the image plane.

26. A solid state imaging device according to Claim 21, wherein all pixels of said array of pixels are reset simultaneously and are read out simultaneously.

27. A solid state imaging device according to Claim 21, wherein said at least one store circuit comprises a plurality of store circuits, with a store circuit corresponding to each pixel and comprising:

a first store circuit for storing a reset value; and

a second store circuit for storing a read out value, with the read out value of a given pixel being modified by the stored reset value for that pixel.

28. A solid state imaging device according to Claim 27, wherein each store circuit further comprises:

a third store circuit for storing a second reset value, with a current reset value and a current read out value being processed simultaneously based upon application of a new reset pulse.

29. A solid state imaging device according to Claim 28, wherein said readout electronics further comprises:

a differential amplifier connected to said first, second and third store circuits; and

a reset circuit for placing said differential amplifier in a common mode reset state prior to reading a signal.

30. A method for making a solid state imaging device comprising:

defining an image plane using a two-dimensional array of pixels; and

placing readout electronics laterally adjacent the image plane for reading signals from the array of pixels, the

readout electronics comprising at least one store circuit.

31. A method according to Claim 30, further comprising connecting a multiconductor signal bus between the array of pixels and the readout electronics.

32. A method according to Claim 30, further comprising forming each pixel using a photosensitive diode, and a switching circuit connected thereto for resetting and discharging the diode.

33. A method according to Claim 32, wherein the switching circuit comprises a first transistor for applying a reset pulse, and a second transistor for connecting the diode to a conductor within the multiconductor signal bus.

34. A method according to Claim 30, wherein the multiconductor signal bus comprises a plurality of stacked conductors.

35. A method according to Claim 30, wherein the readout electronics are placed laterally adjacent one side of the image plane.

36. A method according to Claim 30, wherein the readout electronics are placed laterally adjacent two opposing sides of the image plane.

37. A method according to Claim 30, wherein the image device is configured so that all pixels of the array of pixels are reset simultaneously and are read out

simultaneously.

38. A method according to Claim 30, wherein the at least one store circuit comprises a plurality of store circuits, with a store circuit corresponding to each pixel and comprising a first store circuit for storing a reset value, and a second store circuit for storing a read out value, with the read out value of a given pixel being modified by the stored reset value for that pixel.

39. A method according to Claim 38, wherein each store circuit further comprises a third store circuit for storing a second reset value, with a current reset value and a current read out value being processed simultaneously based upon application of a new reset pulse.

40. A method according to Claim 39, further comprising:

connecting a differential amplifier to the first, second and third store circuits; and

connecting a reset circuit to the differential amplifier for placing the differential amplifier in a common mode reset state prior to reading out a signal.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the

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statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached paper is captioned "Version With Markings to Show Changes Made."

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at page 4, lines 22-29 have been amended as follows:

[The invention and preferred features thereof are defined in the appended Claims.

Briefly stated, the invention is based upon locating the readout electronics off the image plane of the device. In preferred forms of the invention, this is facilitated by connecting each pixel to its associated readout electronics via a multi-conductor signal bus.]

In view of the foregoing background, this and other objects, advantages and features of the present invention are provided by a solid state imaging device comprising a two-dimensional array of pixels defining an image plane, and readout electronics comprising at least one store circuit laterally adjacent the image plane for reading signals therefrom in a predetermined manner.

The invention is based upon locating the readout electronics off the image plane of the device. In preferred forms of the invention, this is facilitated by connecting each pixel to its associated readout electronics via a multiconductor signal bus. The readout electronics may be laterally adjacent one side of the image plane, are they may be laterally adjacent opposing sides of the image plane.

Each pixel preferably comprises a photosensitive diode, and a switching circuit for resetting and discharging the diode. The switching circuit may includes a first transistor for applying a reset pulse, and a second transistor for connecting the diode to a conductor within the

multiconductor signal bus.

The at least one store circuit preferably comprises a plurality of store circuits, with a store circuit corresponding to each pixel. Each store circuit may comprise a first store circuit for storing a reset value, and a second store circuit for storing a read out value. The read out value of a given pixel may be modified by the stored reset value for that pixel. A third store circuit stores a second reset value, with a current reset value and a current read out value being processed simultaneously based upon application of a new reset pulse.

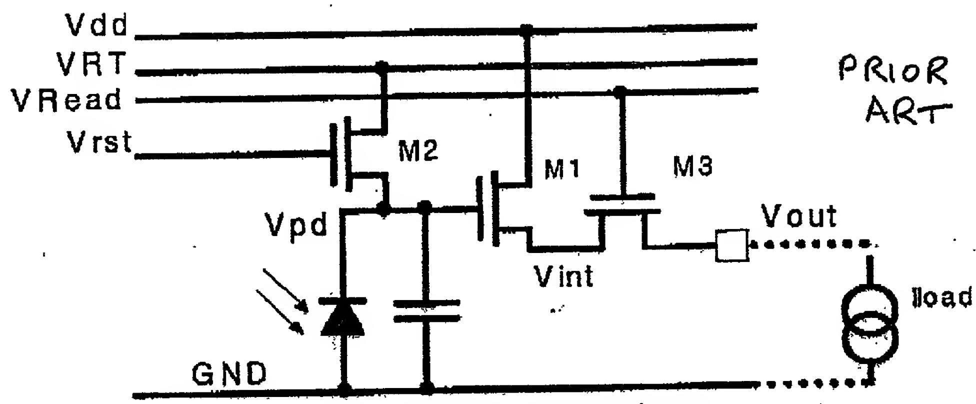

Figure 1 Three Transistor Pixel

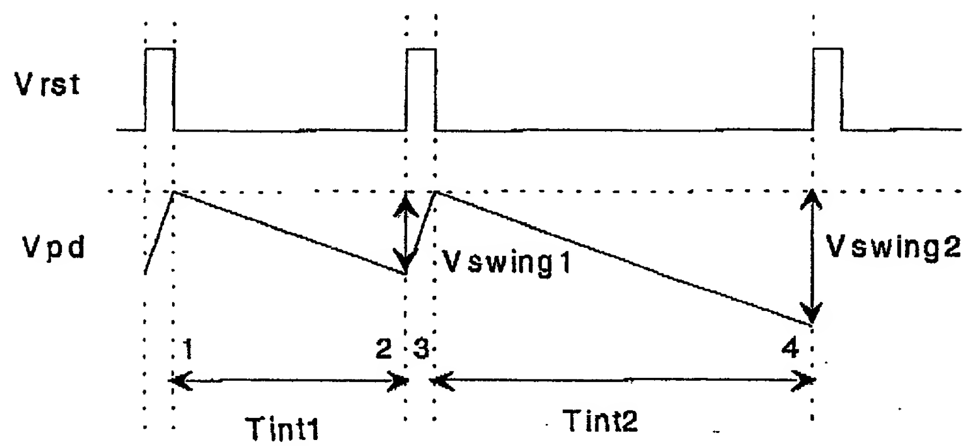

Figure 2 Voltage Swing on Photodiode
(Prior Art)

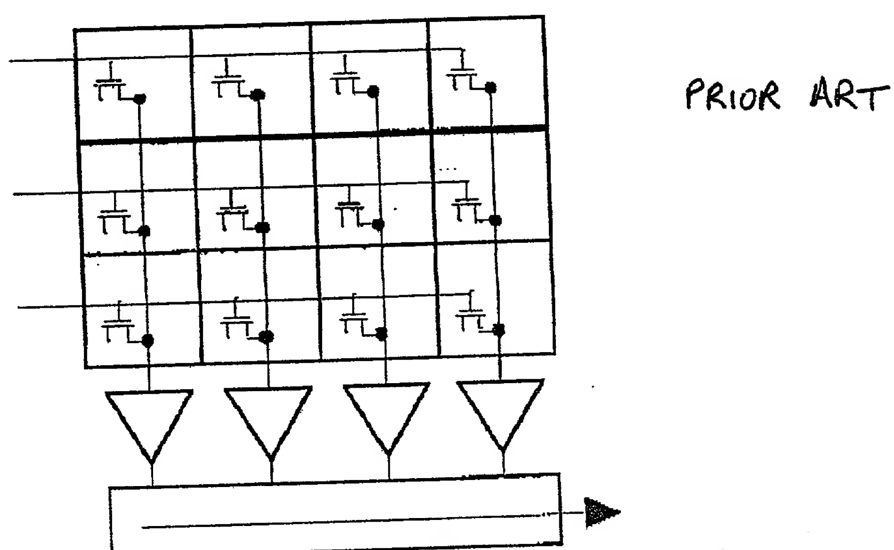

Figure 3 Multiplex Readout

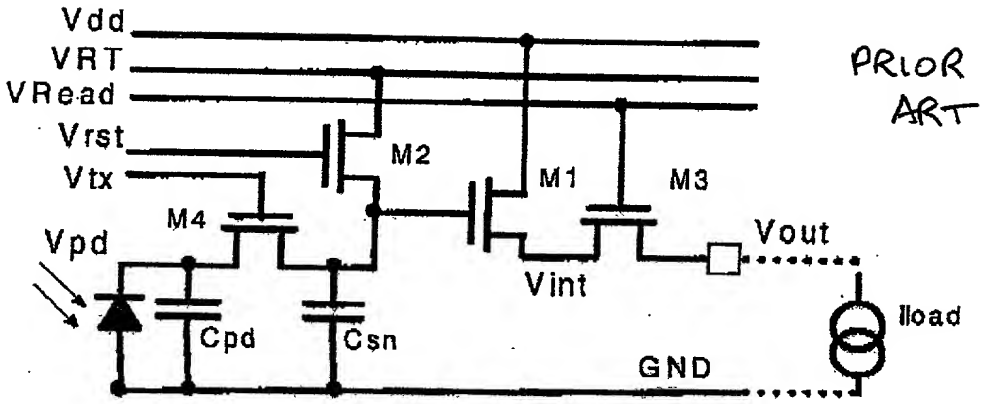

Figure 4 Four Transistor Pixel

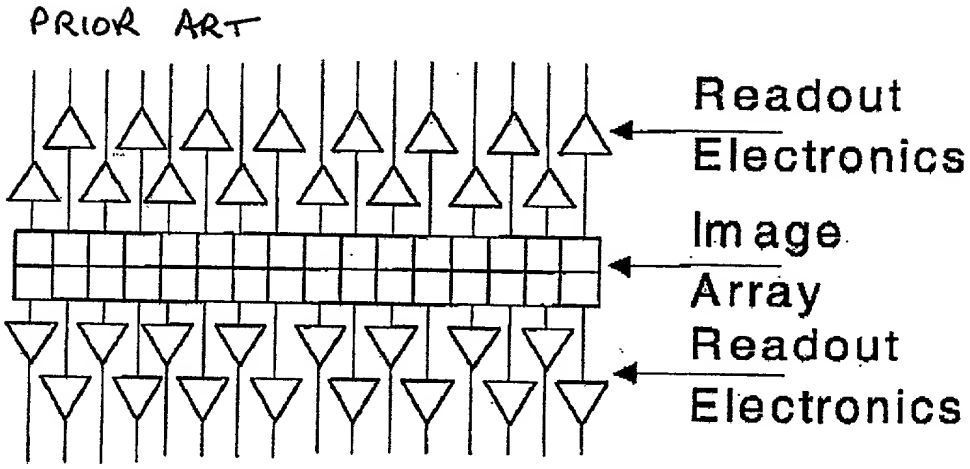

Figure 5 Sophisticated Linear Array

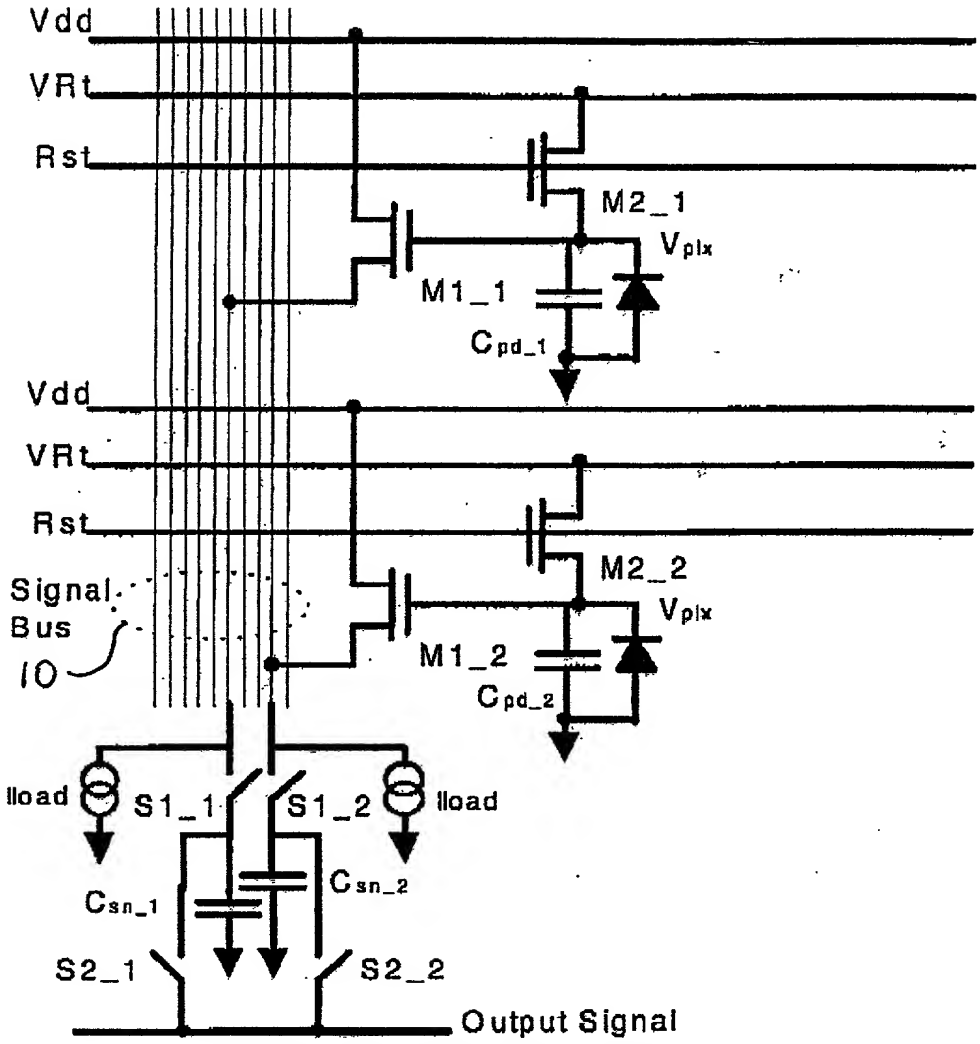

Figure 6 (Part of) New Column Structure

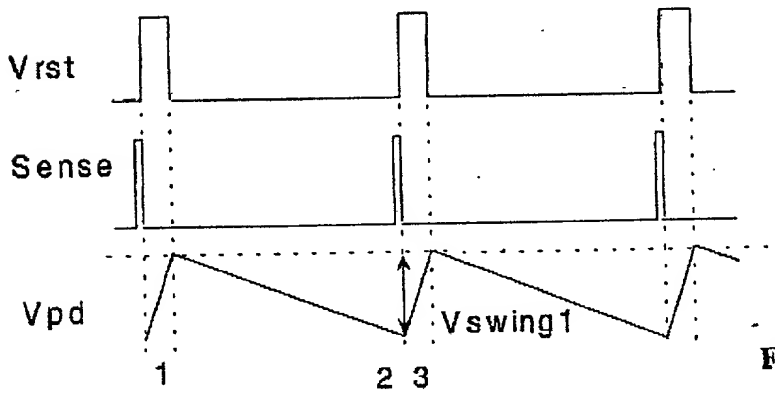

Figure 7 Timing Diagram

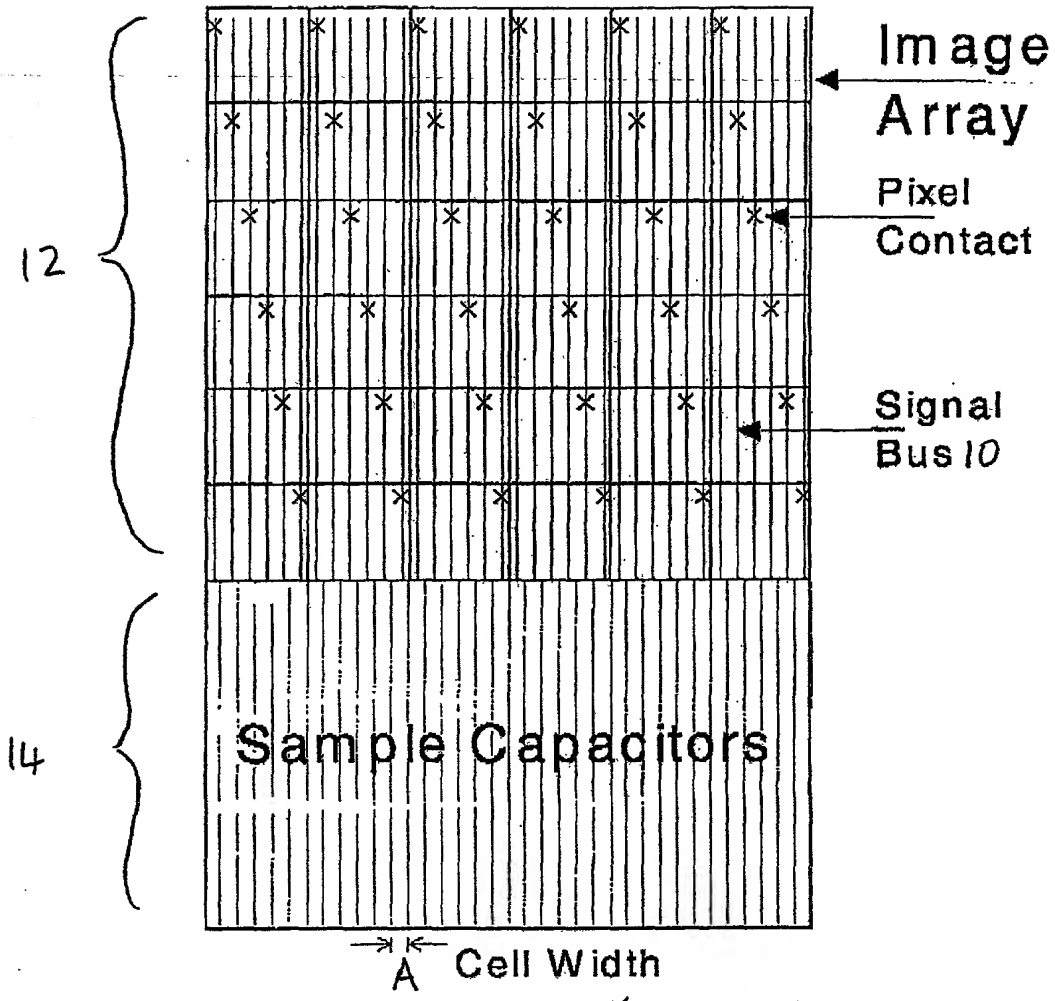

Figure 8 Typical System Layout

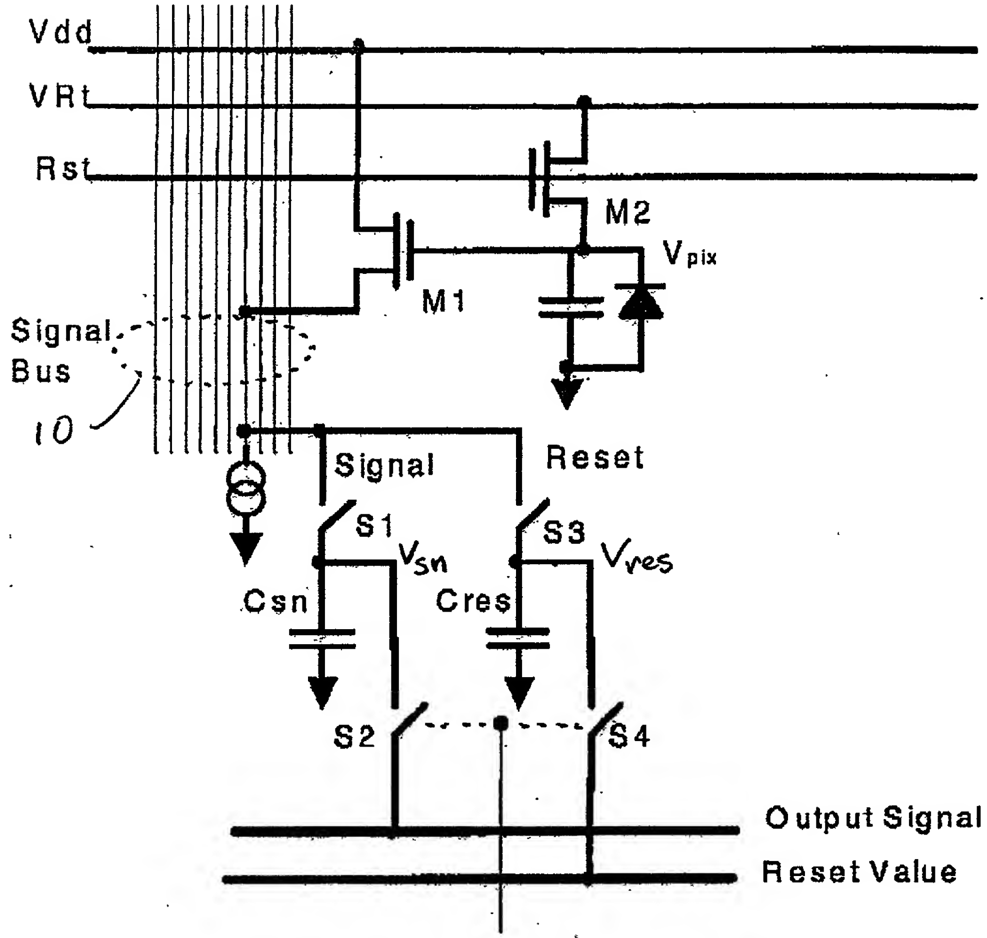

Figure 9 ~~Improved Circuit - Offset Cancellation~~

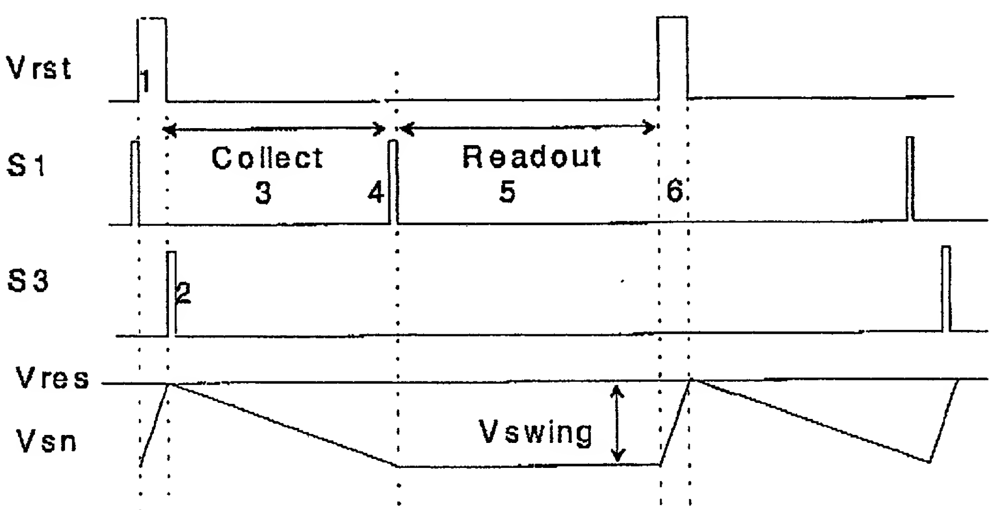

Figure 10 ~~Offset Cancellation - Timing diagram~~

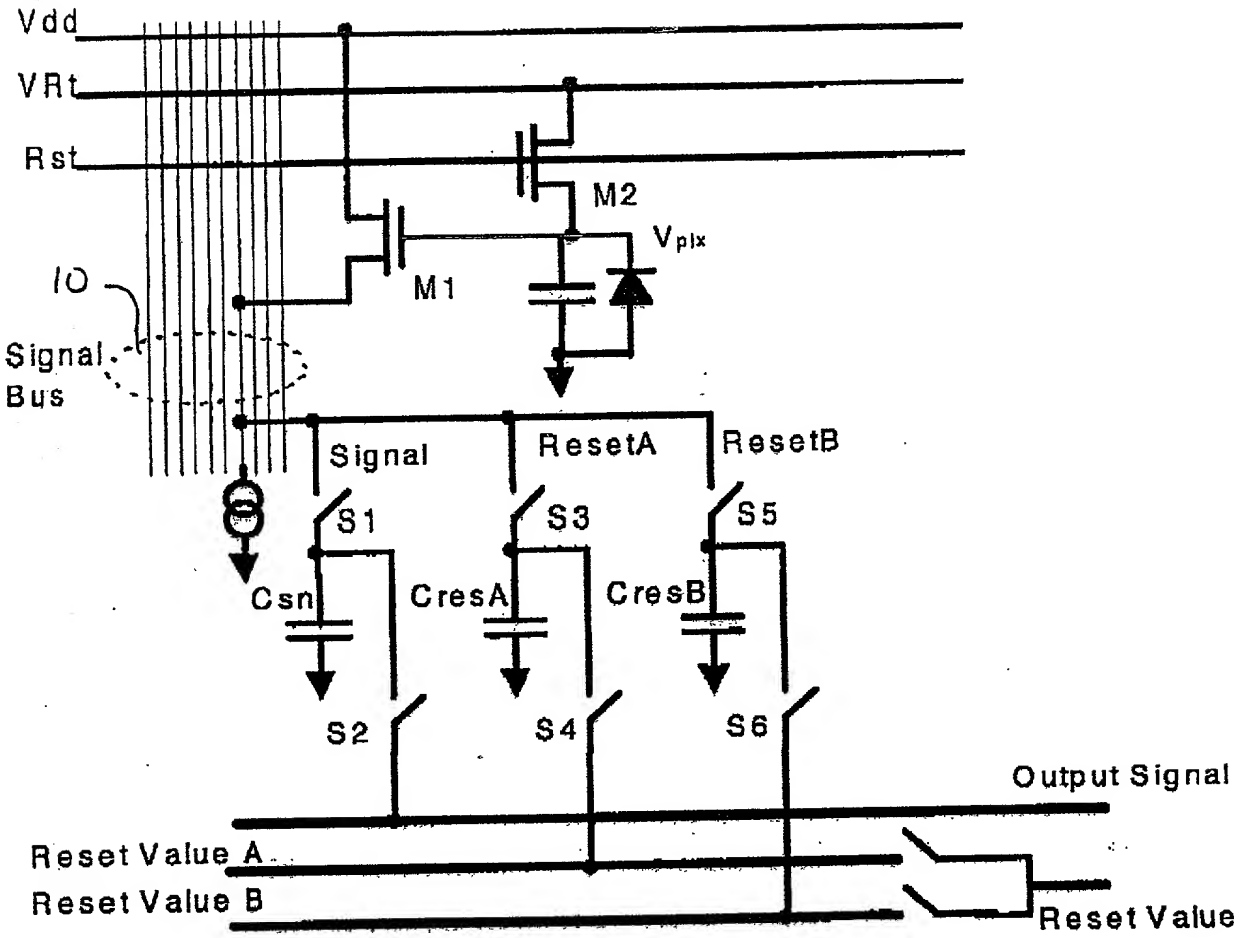

Figure 11 Improved Circuit - Offset Cancellation 2

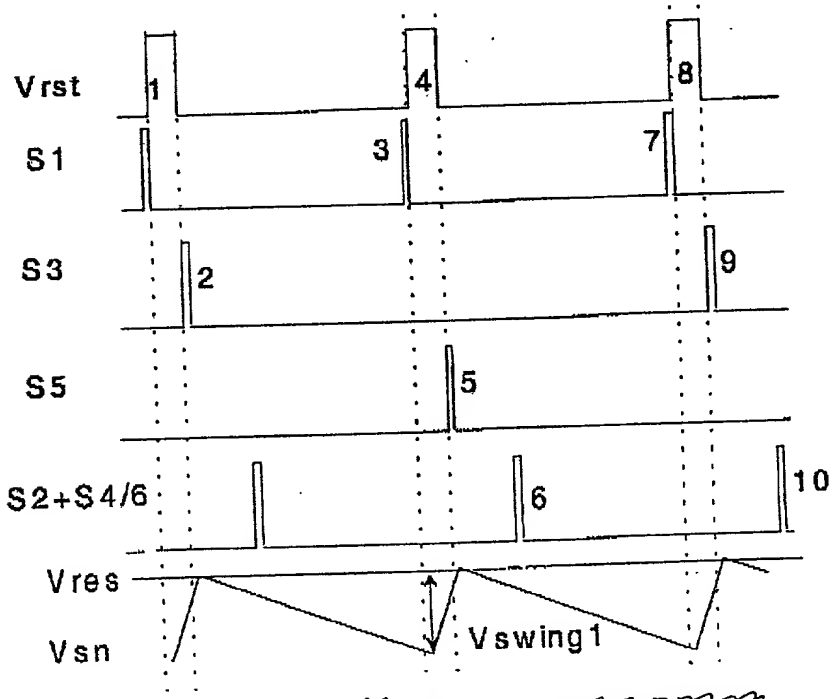

Figure 12 Offset Compensation 2 - Timing Diagram

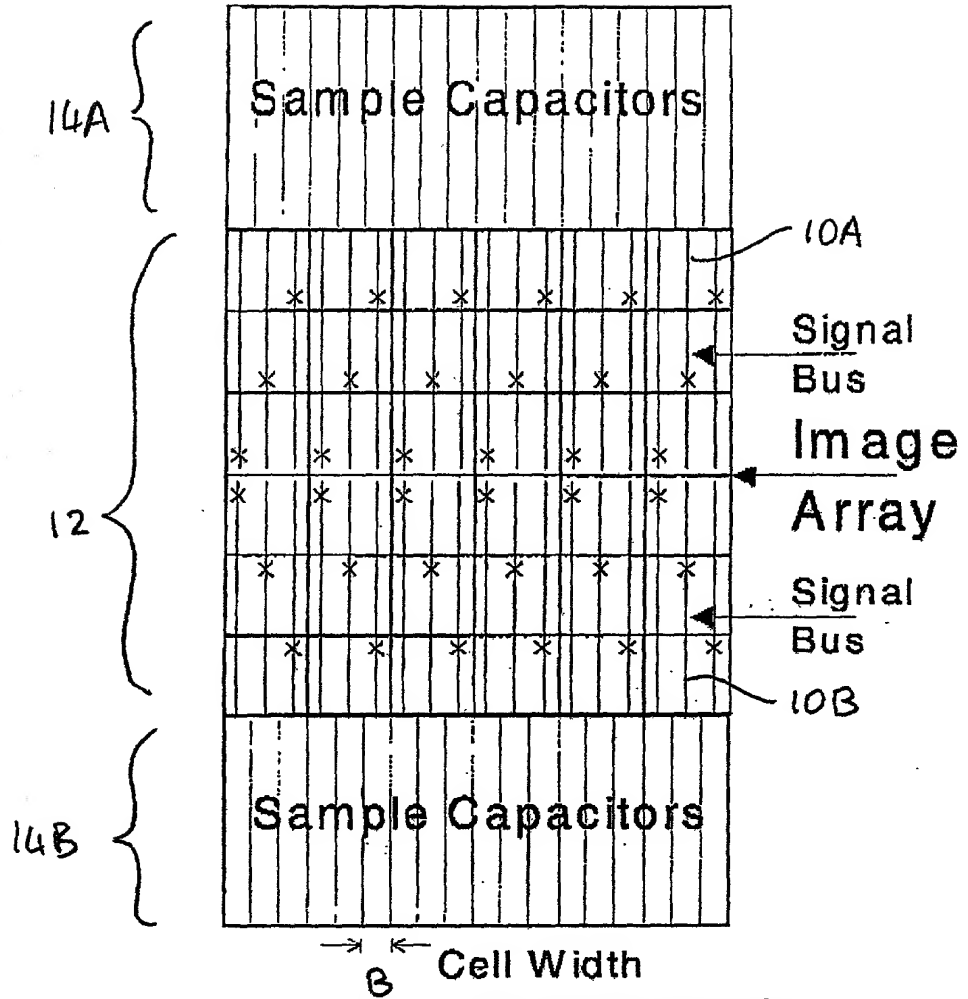

Figure 13 Improved Layout Technique

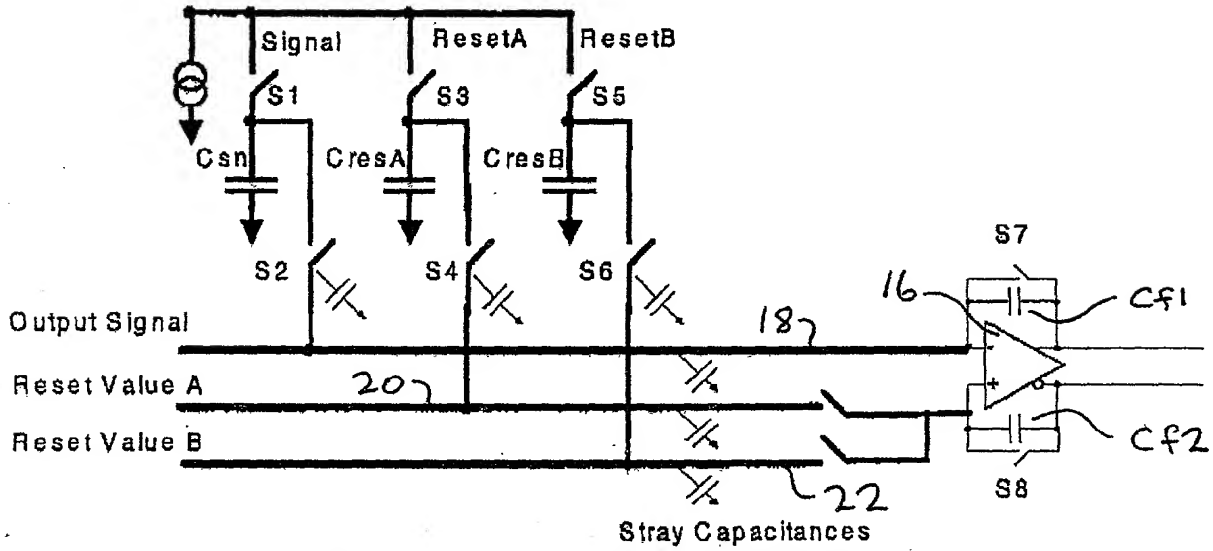

Figure 14 Preferred Readout Amplification